WHAT IS CLAIMED IS:

1. A frequency synchronization apparatus for an orthogonal frequency division multiplexing (OFDM) communication system comprises:

a radio frequency (RF) receiving module for receiving OFDM signal;

an analog/digital (A/D) converter connected to the RF receiving module, the A/D converter converting the OFDM signal into a digital signal;

a frequency synchronization module connected to the A/D converter, the frequency synchronization module synchronizing carrier frequency;

a Fast Fourier Transformer (FFT) connected to the frequency synchronization module, the FFT performing fast Fourier transformation to symbols from the frequency synchronization module;

a channel estimation module connected to the FFT, the channel estimation module estimating carrier channel;

an equalizer connected to the FFT and the channel estimation module, the equalizer equalizing channel;

a residual phase tracking module connected to the equalizer, the residual phase tracking module tracking residual phase;

a demodulator connected to the residual phase tracking module, the demodulator demodulating; and

a controller connected to the frequency synchronization module, the controller controlling the frequency synchronization module.

2. A frequency synchronization apparatus of claim 1 wherein if the received signal contains both short and long training signals, the frequency

synchronization means estimates the frequency offset of the short training signal so as to compensate the long training signal with the frequency offset of the short training signal in a coarse mode, and re-estimates the frequency offset of the compensated long training signal so as to re-compensate the long training signal in a fine mode.

3. A frequency synchronization apparatus of claim 1 wherein if the received signal contains one of both short and long training signal, the frequency synchronization module estimates frequency offset of the training signal and compensates the training signal and data symbol with the estimated frequency offset.

4. A frequency synchronization apparatus of claim 2 wherein frequency synchronization means compensates the data symbol with a sum of the frequency offsets estimated in the coarse and fine modes.

5. A frequency synchronization apparatus of claim 1 wherein the frequency synchronization module comprises:

an estimation submodule 310 for estimating frequency offset and residual phase of a received signal;

a first demultiplexer 330 for selectively outputting the frequency offset and residual phase estimated in the estimation submodule;

an adder 340 for adding the frequency offsets from the first demultiplexer;

a frequency offset compensation submodule for compensating the received signal and data symbol using the frequency offsets from the first demultiplexer and the adder; and

a second demultiplexer for selectively outputting compensated signal from the frequency offset compensation submodule.

6. A frequency synchronization apparatus of claim 5 wherein the estimation submodule comprises;

a shift register part for delaying a sample of the training signal and outputting conjugate complex numbers of a predetermined training signal and a following training signal at the same time; and

a selective estimation part for estimating frequency offset of a signal from the shift register part and residual phase of a signal from the residual phase tracking module.

7. A frequency synchronization apparatus of claim 6 wherein the selective estimation part comprises:

a first multiplier for multiplying the conjugate complex numbers of the signal from the shift register part or the residual phase tracking module;

a first accumulator for accumulating samples obtained by multiplication of the conjugated complex numbers at the first multiplier;

a divider for generating arctangent table address on the basis of a ratio of a real part to an imaginary part of a value accumulated at the first accumulator;

an arctangent table stored arctangent values sampled in a predetermined interval for outputting a corresponding arctangent value to the arctangent table address generated by the divider;

a phase converter for converting the arctangent value into a value of a corresponding region by referring to a sign of the accumulated value at the first accumulator and outputting the value as an estimated frequency offset.

8. A frequency synchronization apparatus of claim 7 wherein the arctangent table is constituted by classifying the arctangent values into predetermined regions and storing the values in a representative one of the regions as representative values.

9. A frequency synchronization apparatus of claim 5 wherein the frequency offset compensation submodule comprises:

a bit expander for sampling the estimated frequency offset;

a second accumulator for generating first log function table address by accumulating frequency offset of each sample obtained at the bit expander;

a first region controller for converting the first log function table address into a corresponding address value in a predetermined region by referring to a sign of value at the bit expander;

a first log function table for outputting a previously stored log function value according to the address value from the first region controller; and

a second multiplier for compensating frequency offset by multiplying the training signal or the data symbol by the log function value from the first log

function table.

10. A frequency synchronization apparatus of claim 9 wherein the first log function table is formed in such a manner of dividing sine and cosine values into predetermined regions and storing values in one of the regions as representative values corresponding to the values in other regions.

11. A frequency synchronization apparatus of claim 10 wherein the first region controller outputs an address value resulting from a subtraction of a predetermined value from an output value and then shift the present region to a next region if the output value is greater than the predetermined value.

12. A frequency synchronization apparatus of claim 10 wherein the first region controller performs complementary operation with the output value of the second accumulator for obtaining a sine or cosine value in the representative region.

13. A frequency synchronization apparatus of claim 1 wherein the residual phase tracking submodule 600 comprises:

a pilot extractor for extraction a pilot signal from a data symbol transformed by the FFT and sending the pilot signal to the selective estimation part;

a residual phase compensation part 620 for compensating the data symbol with the residual phase of the data symbol estimated at the selective

estimation part.

14. A frequency synchronization apparatus of claim 13 wherein the residual phase compensation part comprises:

a second region controller 621 for outputting a second log function table address corresponding to the residual phase value from the first demultiplexer 330;

a second log function table 663 for outputting a previously stored log function value corresponding to the log function table address from the second region controller; and

a third multiplier 623 for compensating the residual phase by multiplying the log function value from the second log function table with the compensated data symbol.

15. A frequency synchronization apparatus of claim 14 wherein the second log function table is formed in such a manner of dividing sine and cosine values into predetermined regions and values in one of the regions are stored as representative values corresponding to the values in other regions

16. A frequency synchronization apparatus of claim 15 wherein the second region controller outputs an address value resulting from a subtraction of a predetermined value from an output value and then shift the present region to a next region if the output value is greater than the predetermined value.

17. A frequency synchronization apparatus of claim 16 wherein the second region controller performs complementary operation with the output value of the second accumulator for obtaining a sine or cosine value in the representative region.

18. A frequency synchronization method for an orthogonal frequency division multiplexing (OFDM) communication system comprising the steps of:

(a) estimating frequency offset of training signal;

(b) compensating frequency of the training signal with the estimated frequency offset;

(b) performing fast Fourier transformation on the frequency;

(c) estimating channel of the transformed frequency;

(d) compensating a data symbol of an input signal with the frequency offset estimated at step (b);

(e) performing fast Fourier transformation on the data symbol;

(f) compensating the data symbol with the channel estimated at step (c);

(g) tracking a residual phase of the estimated data symbol; and

(h) compensating the residual phase.

19. A frequency synchronization method of claim 18 wherein the step (a) comprises the sub-steps of, if the training signal has short and long training signals,

(a1) estimating the frequency offset using the short training signal;

(a2) compensating the long training signal with the estimated frequency offset of the short training in a coarse mode;

(a3) estimating a frequency offset of the long training signal compensated at the sub-step (a2); and

(a4) re-compensating the long training signal compensated at the sub-step (a2) with the frequency offset estimated at the sub-step (a3) in a fine mode.

20. A frequency synchronization method of claim 19 wherein the data symbol is compensated with a sum of the frequency offsets estimated in the fine and coarse modes.

21. A frequency synchronization method of claim 19 wherein the sub-step (a1) comprises the stages of:

(a1-1) delaying a sample of the short training signal;

(a1-2) outputting conjugate complex numbers of a present training signal and a following training signal at the same time;

(a1-3) multiplying the conjugate complex numbers of the short training signal;

(a1-4) accumulating samples obtained by multiplication of the stage (a1-3);

(a1-5) generating an arctangent table address on the basis of a ratio of a real and imaginary parts of an accumulated value at the stage (a1-4);

(a1-6) referring to a sign of the accumulated value;

(a1-7) converting an arctangent value stored in the arctangent table

address of an arctangent table generated at the stage (a1-5) into a value in a corresponding region; and

(a1-8) outputting the value as an estimated frequency offset.

22. A frequency synchronization method of claim 21 wherein the sub-step (a2) comprises the stages of:

(a2-1) sampling the estimated frequency offset in a predetermined size;

(a2-2) accumulating samples;

(a2-3) generating a first log function table address on the basis of the accumulated value;

(a2-4) referring to a sign of the accumulated value;

(a2-5) converting an first log function table address into an address in a corresponding region; and

(a2-6) outputting a log function value stored at the converted address.

23. A frequency synchronization method of claim 22 wherein the log function value at the stage (a2-6) is multiplied with the long training signal.

24. A frequency synchronization method of claim 21 wherein the arctangent table is constituted by classifying the arctangent values into predetermined regions and storing the values in a representative one of the regions as representatives.

25. A frequency synchronization method of claim 22 wherein the log

function value is outputted after complementary operation for obtaining a sine or cosine value in symmetrical regions.

26. A frequency synchronization method of claim 22 wherein the first log function table is formed in such a manner of dividing sine and cosine values into predetermined regions and values in one of the regions are stored as representative values corresponding to the values in other regions.

27. A frequency synchronization method of claim 22 wherein an address value resulting from a subtraction of a predetermined value from an output value is outputted and then the present region is shifted to a next region if the output value is greater than the predetermined value.

28. A frequency synchronization method of claim 22 wherein the sub-step (a3) comprises the stages of:

(a3-1) delaying a sample of the compensated long training signal;

(a3-2) outputting conjugate complex numbers of a present long training signal and a following training signal at the same time;

(a3-3) multiplying the conjugate complex numbers of the long training signal;

(a3-4) accumulating samples obtained by multiplication of the stage (a3-3);

(a3-5) generating an arctangent table address on the basis of a ratio of a real and imaginary parts of the accumulated value at stage (a3-4);

(a3-6) referring to a sign of the accumulated value;

(a3-7) converting the arctangent value stored in the arctangent table address of the arctangent table generated at the stage (a3-5) into a value in a corresponding region; and

(a3-8) outputting the value as an estimated frequency offset.

29. A frequency synchronization method of claim 28 wherein the sub-step (a4) comprises the stages of:

(a4-1) sampling the estimated frequency offset in a predetermined size;

(a4-2) accumulating samples;

(a4-3) generating a log function table address on the basis of the accumulated value;

(a4-4) referring to a sign of the accumulated value;

(a4-5) converting a first log function table address into an address in a corresponding region;

(a4-6) outputting a log function value stored at the converted address.

30. A frequency synchronization method of claim 29 wherein the log function value at the stage (a4-6) is multiplied with the long training signal.

31. A frequency synchronization method of claim 28 wherein the arctangent table is constituted by classifying the arctangent values into predetermined regions and storing the values in a representative one of the regions as representatives.

32. A frequency synchronization method of claim 29 wherein the log function value is outputted after complementary operation for obtaining a sing or cosine value in symmetrical regions.

33. A frequency synchronization method of claim 29 wherein the first log function table is formed in such a manner of dividing sine and cosine values into predetermined regions and values in one of the regions are stored as representative values corresponding to the values in other regions.

34. A frequency synchronization method of claim 29 wherein an address value resulting from a subtraction of a predetermined value from an output value is outputted and then the present region is shifted to a next region if the output value is greater than the predetermined value.

35. A frequency synchronization method of claim 18 wherein the step (g) comprises the sub-steps of:

(g1) extracting a pilot signal from the compensated data symbol;

(g2) performing a conjugate complex number multiplication;

(g3) accumulating samples obtained by the multiplication of the sub-step (g2);

(g4) generating an arctangent table address on the basis of a ratio of a real and imaginary parts of an accumulated value at the stage (g3);

(g5) referring to a sign of the accumulated value;

(g6) converting an arctangent value stored in the arctangent table address of an arctangent table generated at the stage (g4) into a value in a corresponding region;

(g7) outputting the value as an estimated residual phase;

(g8) generating a second log function table address according to the estimated residual phase;

(g9) outputting a log function value corresponding to the second log function table address; and

(g10) multiplying the log function value with the data symbol.

36. A frequency synchronization method of claim 35 further comprises a sub-step of classifying the arctangent values into predetermined regions and storing the values in a representative one of the regions as representative values.

37. A frequency synchronization method of claim 35 further comprises a sub-step of dividing sine and cosine values into predetermined regions and storing values in one of the regions as representative values corresponding to the values in other regions.

38. A frequency synchronization method of claim 35 further comprises a sup-step of outputting an address value resulting from a subtraction of a predetermined value from an output value and shifting the present region to a next region if the output value is greater than the predetermined value.

39. A frequency synchronization method of claim 35 further comprises the sub-step of outputting sine and cosine values after performing complementary operation with the log function value for obtaining sine or cosine value in symmetrical regions.